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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,503	03/08/2004	Li-Sheng Chen	21541-000310	2502

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EXAMINER	
LIN, WEN TAI	

ART UNIT	PAPER NUMBER
2154	

NOTIFICATION DATE	DELIVERY MODE
11/29/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-INBOX@AKACHANLAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/708,503	CHEN ET AL.	
	Examiner	Art Unit	
	Wen-Tai Lin	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/8/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *10-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/8/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 are presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to implementation of network traffic management tasks on signal processors, classified in class 709, subclasses 224.

II. Claims 10-16 and 44, drawn to digital signal processing architecture, classified in class 712, subclass 35.

III. Claims 17-30, drawn to flow control of data transmission through a network, classified in class 370, subclass 235.

IV. Claims 31-43, drawn to inter-program communication using shared memory, message or event notification such as interruption, classified in class 719, subclasses 312.

3. The inventions are distinct, each from the other because:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such

as components in digital signal processing integrated circuit and how it interacts with a network processor as a data/event driven processor. See MPEP 806.05(d).

4. The inventions are distinct, each from the other because:

Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as data congestion flow control in particular when the network traffic flows are differentiated in terms of class of service. See MPEP 806.05(d).

5. The inventions are distinct, each from the other because:

Inventions I and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention IV has separate utility such as inter-program communication (within same clock domain) using shared memory represented as flag, mailbox memory location etc. See MPEP 806.05(d).

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

7. A telephone call was made to Mr. Melvin Chan at (408) 701-0035 on November 19, 2007 to request an oral election to the above restriction requirement. A provisional election was made without traverse to prosecute the invention of Group I, claims 1-9. Affirmation of this election must be made by applicant in responding to this office action. Claims 10-44 are withdrawn from further consideration by the examiner as being drawn to a nonelected invention. See 37 CFR 1.142(b).

8. Claims 1-9 are presented for examination.

9. Applicant is reminded to update the statuses of the applications listed in the specification.

10. Claims 3-4 are objected to because the term "the channel" in claim 3 appears to lack antecedence basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.(hereafter "Lee")[U.S. PGPub 20030152084].

12. As to claims 1-2, Lee teaches the invention substantially as claimed including: a method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory [e.g., paragraphs 19 and 74-75; i.e., each MISD processor has 32 x 64K bytes of instruction memory and 64K registers];

performing a policing function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit [e.g., 220a, Fig. 4, paragraph; 76, wherein the first MISD processor (PCU) performs traffic policing];

performing a congestion control function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core [e.g., 220b, Fig.4 (i.e., TPU); paragraph 76; note that result of process 222a is fed to its following process 222b]; and

performing a shaping function in a fourth core of the digital signal processing integrated circuit, wherein the fourth core processes data generated by the third core [e.g., 220c (i.e., FPU), Fig.4; paragraph 76].

Lee teaches that the scheduling function in the second core of the digital signal processing integrated circuit together with the congestion control function [paragraph

76]. Lee does not suggest performing the scheduling function in a separate core (i.e., the third core of the digital signal processing integrated circuit).

However, based on Lee's modular MISD arrangement, it is obvious to one of ordinary skill that the system may be extended to more than the three-stage processors (as illustrated in Fig. 4). For example, when it is perceived that traffic scheduling takes up a big chunk of processing time the MISD a different MISD processor, an ordinary skilled artisan could have dedicated a third MISD in the pipe for the job because the approach is predictable and the advantage of alleviating processing bottle-neck using additional MISD is obvious. See KSR, 127 S. Ct. at 1742, 82 USPQ2d at 1397.

Further, Lee does not specifically teach that the four-stage MISD processors are implemented in a digital signal processing integrated circuit.

However, it is well known, at the time the invention was made, that advanced IC fabrication technology could fit multi-million-transistors on a single chip. High density interconnection technology to integrate multiple processor dies onto a single integrated chip package is also available. It would have been obvious to one of ordinary skill in the art to have integrated Lee's four MISD processors into a single digital signal processing circuit because it reduces the overall physical size of the processors and parasitic capacity due to wirings (i.e., potentially makes the system running at a higher speed).

13. As to claim 3, Lee further teaches that a traffic management function comprises sorting the traffic by class of service, policing traffic to not exceed boundary of a

bandwidth of the channel, and scheduling traffic [e.g., paragraphs 24-25 and 76; Fig. 38] .

14. As to claim 4, Lee further teaches that the scheduling traffic is based on priority queuing, first in first out queuing, class based queuing, round robin, waiting round robin, earlier deadline first, weighted fair queue, deficit round robin, or modified deficit round robin [e.g., paragraphs 261 & 344; note that inherently a queue is order as first-in-first-out].

15. As to claim 5, Lee further teaches that there is no direct communication path between the first core and the second core [e.g., paragraphs 83-84, i.e., the MISD processors are interconnected through buffers or external memory].

16. As to claim 6, Lee further teaches that the data generated by the first core is passed to the second core using a mailbox [e.g., paragraph 84, i.e., "the DBU 292 stores the fixed size buffers into memory and other functional units (such as the FPU) have access to those buffers."].

17. As to claims 8-9, since the features of these claims can also be found in claims 2, they are rejected for the same reasons set forth in the rejection of claims 2 above.

18. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.(hereafter "Lee")[U.S. PGPub 20030152084], as applied to claims 1-6 and 8-9 above, further in view of Bass et al.(hereafter "Bass")[U.S. Pat. No. 6769033].

19. As to claim 7, Lee does not specifically teach the first core and second core are synchronized using an interrupt mechanism with a plurality of timers.

However, in the same field of endeavor, Bass teaches synchronizing the passing of frames among the processors by monitoring input events, Data Buffers available for dispatch, Interrupts and Timers [e.g., col. 9, lines 31-32; col. 21, line 62- col. 22, line 5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a plurality of timers for triggering Lee's data passing between MISD processors because: (1) interrupt is a well known technique for causing event triggering and response; (2) using a plurality of timers that are implemented local to each processor avoid the use of a global timer and the associated problem of slower timing and clock skew; and (3) Lee teaches using the expiration of a timer to cause the reading of some data entries [paragraphs 200-201], a scheme similar to Bass's use of timer and interrupt for data passing.

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Hogg et al. [U.S. Pat. No. 7266122];

Lee et al. [U.S. Pat. No. 6996117];

Vanhoof et al. [U.S. Pat. No. 7099949];

Johnson et al. [U.S. PGPub 20020049841]; and

Greenblat et al. [U.S. Pat. No. 7103008].

21. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 days from the mail date of this letter. Failure to respond within the period for response will result in ABANDONMENT of the application (see 35 U.S.C. 133, M.P.E.P. 710.02, 710.02(b)).

Conclusion

Examiner note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the contest of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Tai Lin whose telephone number is (571)272-3969. The examiner can normally be reached on Monday-Friday(8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(571) 273-8300 for official communications; and

(571) 273-3969 for status inquires draft communication.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Tai Lin

November 23, 2007

Wen-Tai Lin

11/23/07